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Research and design of PFC control based on DSP

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Abstract. A realization scheme of single-phase power factor correction (PFC) circuit based on digital signal processor (DSP) is proposed and discussed. The parameters of the main circuit, signal conditioning circuit, current loop and voltage loop of PI control are designed. Finally, a prototype of the system is built and the actual measured results show that the power factor is above 0.99 at full load.

Key words. PFC, DSP, current loop, voltage loop, PI control.

1. Introduction

With the development of power electronic technology and wide application of power electronic devices in various areas, the current harmonic problem of the power grid is increasingly serious, and the harmonic pollution brings a series of harm not only to the system itself, but also to the surrounding electromagnetic environment [1]. The power factor correction (PFC) can effectively eliminate the harmonics of the rectifier, so it has a wide range of applications. Now, with the development of digital control technology, more and more control strategies is realized through digital signal processors (DSP) [2].

TMS320LF2406 is a kind of a low-price and high-performance chip introduced by TI company. Its processing ability is 30 MIPS, which is suitable for the control system of the motor and power supply transformation. Taking the widely used Boost-PFC circuit as an example, the current loop and voltage loop circuits are designed, using the TMS320LF2406 digital chip. Finally, a prototype is built, and the ideal dynamic and steady-state results are obtained in a practical application.

The basic parameters of the system are: output power $P_{\text{out}} = 800\,\text{W}$, input AC voltage range is $180 - 300\,\text{V}$, input voltage frequency is $45 - 65\,\text{Hz}$ and output DC voltage is $415\,\text{V}$.

The scheme of the system is depicted in Fig. 1.

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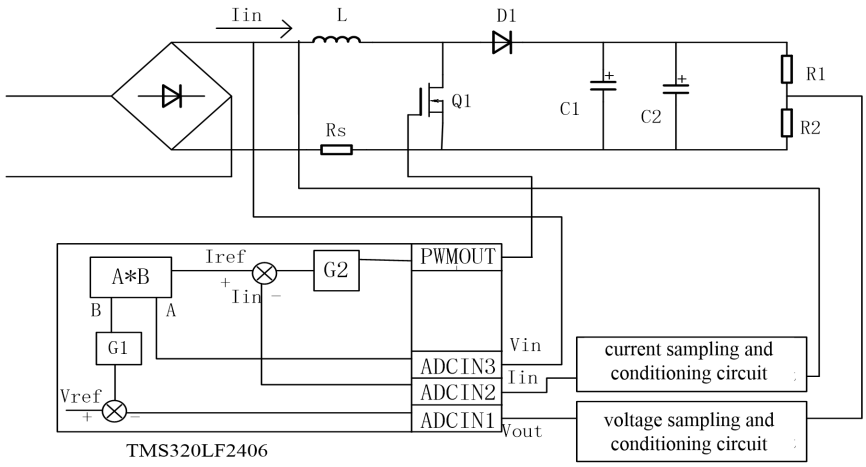

Fig. 1. Block diagram of a PFC converter based on DSP control

The rectified input voltage V_{in}, inductor current I_{in} and DC output voltage V_{out} are transformed, filtered, isolated by the corresponding sample and conditioning circuits, and then they are sent to the ADC module of DSP [3]. The output voltage V_{o} is sampled, then it is compared with the reference voltage V_{ref} and then the offset is sent into the voltage PI controller G1. The output of the voltage loop controller is defined as B, the input voltage is defined as A, and the two parameters are multiplied by the multiplier as the reference current I_{ref} of the current loop [4]. The inductor current I_{in} is compared with the reference signal I_{ref}, and the offset is taken as the input of PI controller of the current loop G2. The output value of current loop is compared with the value of the carrier signal in the DSP, the comparative value is used to change the PWM duty cycle in a switching period, and then through the isolation driving circuit makes the power switch turn-on and turn off [5]. In this way, the average value of the input current can track the input voltage waveform, so that the input current and input voltage are in the same phase, and the output voltage is stable [6].

The main circuit works in the CCM mode of the Boost converter, realizing voltage conversion and power factor correction. The digital control circuit is the core of the system, mainly converting analog signals to digital signals and achieving control algorithm of PI control of the voltage loop and current loop; the output signal is amplified by a switch tube driving circuit, then it is sent to the switch tube of the main circuit to control turn-on and turn-off of the switch tube [7].

2. The control circuit design

The objective of control circuit design is to determine the main circuit parameters [8], PI parameters of the voltage loop and current loop and the structure of signal sampling and conditioning circuits.

In the use of the Bode diagram method, the PI regulator is converted to the problem of zero point setting, only needing to set a reasonable zero, and then according to the ratio of the Bode diagram to determine the value of KP and KI [9].

2.1. The main circuit design

The main circuit inductance is operating in the current continuous mode (CCM). The continuation of the inductor current depends on the output power, switching frequency, inductance size and other parameters. According to the calculation, the value of the inductance is selected 78 μH. The output capacitor C depends on ripple size of the required output voltage, switching frequency, etc. According to the calculation, the design selects two 220 μF electrolytic capacitors. The current sampling resistor R_s is selected 30 MΩ. The PFC principle diagram of the main circuit is shown as Fig. 2.

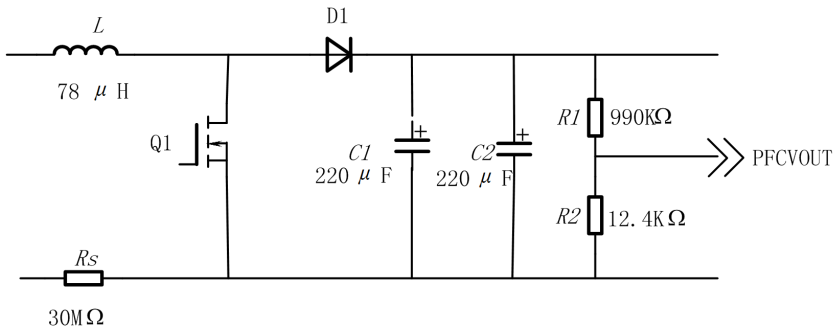

Fig. 2. PFC principle diagram of the main circuit

The switching frequency of the main circuit is selected 80 kHz. In order that the current loop cannot be disturbed by the noise of the switch, at the same time the current loop cannot also be affected by the low bandwidth, otherwise it will affect the effect of the current waveform to follow the voltage waveform [11]. In order to prevent from influencing the bus voltage ripple on the PFC controller, the crossing frequency of the voltage loop is controlled in less than half of the input electric frequency, in this paper, the calculate frequency of the voltage loop is selected 160 kHz/8=20 kHz.

2.2. PFC current loop design

When the PFC inductor current is CCM mode, the dynamic block diagram of the S-field of the PFC current loop is shown in Fig. 3.

Here, V_{Rs} is the voltage on the PFC input current sampling resistor, V_I is the PFC input voltage, V_o is the PFC output DC voltage, D is the duty cycle, L is PFC inductor, R_s is PFC input current sampling resistor. Considering 260 μH inductor of the analog LISN's low frequency impedance characteristic and the differential-mode component of the input filter, the circuit model of the PFC current loop is shown in

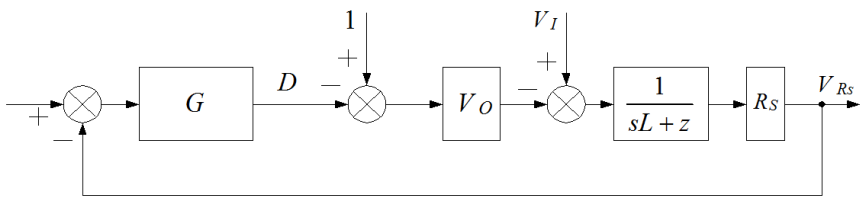

Fig. 3. Dynamic block diagram of S-field of PFC current

Fig. 4 with the source AC power supply.

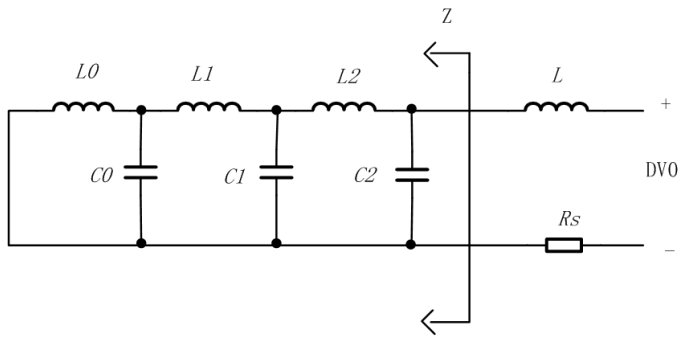

Fig. 4. Circuit model of the PFC current loop considering LISN'S inductor and filter

Here, L is 260 µH inductor of the analog LISN's low frequency impedance characteristic (actual loop test is 0). Symbol C_0 is 2.2 µF capacitor of the module input port, L_1 is 24 µH differential-mode component of input common-mode inductor, C_1 is 0.47 µF capacitor of between input common-mode inductors, L_2 is the sum of 13 µH differential-mode component of input common-mode inductor and 138 µH input differential-mode inductor. Finally, C_2 is 1 µF capacitor placed after the input rectifier.

Assuming that the impedance of the AC source is 0, the calculation formula of impedance Z is as follows:

$$Z = \frac{k_1 s^5 + k_2 s^3 + k_3 s}{k_4 s^6 + k_5 s^4 + k_6 s^2 + 1}\,, \tag{1}$$

where

$$k_1 = L_1 L_2 C_1 L_0 C_0\,, \tag{2}$$

$$k_2 = L_1 L_0 C_0 + L_2 L_0 C_0 + L_2 L_1 C_1 + L_2 L_0 C_1\,, \tag{3}$$

$$k_3 = L_0 + L_1 + L_2\,, \tag{4}$$

$$k_4 = L_1C_1L_2C_2L_0C_0\,, \tag{5}$$

$$k_5 = L_1C_2L_0C_0 + L_2C_2L_0C_0 + L_2C_2L_1C_1 + L_2C_2L_0C_1 + L_1C_1L_0C_0\,, \tag{6}$$

$$k_6 = L_0C_2 + L_1C_2 + L_2C_2 + L_0C_0 + L_1C_1 + L_0C_1\,. \tag{7}$$

Considering the influence of the input filter, the controlled object of the current loop is changed into

$$P_0(s) = \frac{V_{\mathrm{O}}R_{\mathrm{S}}}{sL + Z} = \frac{V_{\mathrm{O}}R_{\mathrm{S}}[k_4s^6 + k_5s^4 + k_6s^2 + 1]}{k_7s^7 + k_8s^5 + k_9s^3 + k_{10}s}\,, \tag{8}$$

where

$$k_7 = L_1C_1L_2C_2L_0C_0L\,, \tag{9}$$

$$\begin{aligned} k_8 = {} & L_1C_2L_0C_0L + L_2C_2L_0C_0L + L_2C_2L_1C_1L + L_2C_2L_0C_1L + \\ & + L_1C_1L_0C_0L + L_1C_1L_0C_0L_2\,, \end{aligned} \tag{10}$$

$$\begin{aligned} k_9 = {} & L_0C_2L + L_1C_2L + L_2C_2L + L_0C_0L + L_1C_1L + L_0C_1L + L_1L_0C_0 + \\ & + L_2L_0C_0 + L_2L_1C_1 + L_2L_0C_1\,, \end{aligned} \tag{11}$$

$$k_{10} = L + L_0 + L_1 + L_2\,. \tag{12}$$

This block diagram is effective in the frequency band between the resonant frequency (860 Hz) of the LC filter in the PFC circuit and switching frequency.

The PFC current signal sampling and conditioning circuit scheme is shown in Fig. 5. The circuit uses a differential amplifier to amplify the circuit, using in series the first-order RC filter with the cut-off frequency of 50 kHz and second-order RC filter with 47 kHz.

Through the analysis, we can derive that the transfer function of the PFC current signal sampling circuit is

$$H(\mathrm{S}) = \frac{8.12}{(3.198 * 10^{-6}\mathrm{s} + 1)(1.122 * 10^{-11}\mathrm{s}^2 + 1.73 * 10^{-5}\mathrm{s} + 1)}\,. \tag{13}$$

The 3V signal in PFC AD sampling port corresponds to the number 1023, while the output digital quantity 2032 of the PFC current loop controller corresponds to the PWM pulse width duty cycle 1, therefore, through the synthesis, the discrete dynamic block diagram of the PFC current loop is shown as Fig. 6, T being the calculation frequency of PFC current loop.

With the calculation frequency of 50 kHz, the Z transform is performed on the

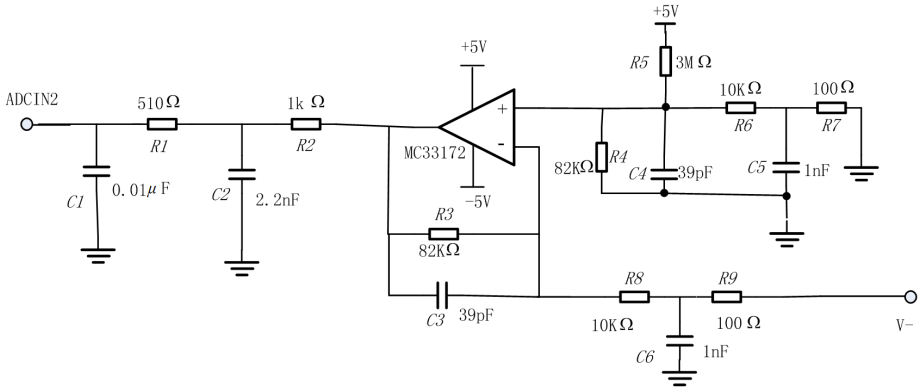

Fig. 5. PFC current signal sampling circuit

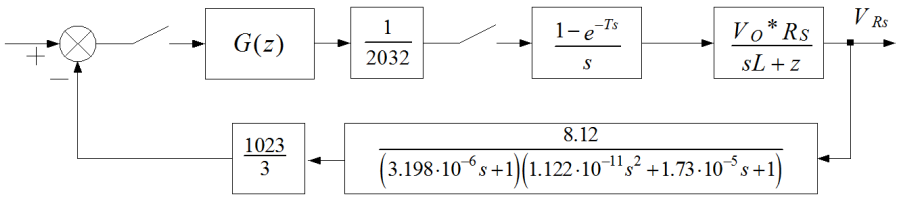

Fig. 6. Discrete dynamic block diagram of PFC current loop

part of the block diagram except the open transfer function. The resultant function is given as

$$P(z) = A(z)/B(z)\,,$$

where

$$\begin{aligned} A(z) &= 0.421z^{-1} + 3.72z^{-2} + 49.1z^{-3} + 42.7z^{-4} - \\ &- 25.4z^{-5} + 56.4z^{-6} + 36.2z^{-7} + 2.71z^{-8}\,, \\ B(z) &= 01 + 9.69z^{-1} + 109z^{-2} - 116z^{-3} + 114z^{-4} - \\ &- 159z^{-5} + 31.3z^{-6} + 9.71z^{-7} + z^{-8}\,. \end{aligned} \tag{14}$$

In order to use frequency analysis method to design, the Z domain can be changed to the W domain based on the bilinear transformation method. The Bode figure of $P(w)$ is shown in Fig. 7 (horizontal coordinate is for frequency, units are rad/s). In order to improve the PFC current inhibition ability on the third and fifth harmonics in the input current to obtain lower THD, PFC current loop controller $G(w)$ must contain an integral part, and the zero point cannot be too far below the cut-off frequency of the open loop transfer of the PFC current loop. Let us assume that after correction the open loop cutoff frequency of the PFC current loop is 5 kHz=$3.14\cdot 10^4$ rad/s. Due to the inherent existence of a calculating cycle delay $T = 12.5$ μs in the digital control, thus, at the 5 kHz frequency the phase lag of $\frac{5k}{80k}\cdot 180° = 11.25°$ is introduced. In order to get a sufficient stability, we can set two zero points for 3 kHz;

at the same time, in order to improve the anti-interference ability of the current loop, we set a pole point in 6 kHz. The structure of the current loop controller in W domain is as follows

$$G(w) = \frac{K * \left(\frac{w}{2\pi \cdot 3k} + 1\right)\left(\frac{w}{2\pi * 3k} + 1\right)}{w\left(\frac{w}{2\pi * 6k} + 1\right)}. \tag{15}$$

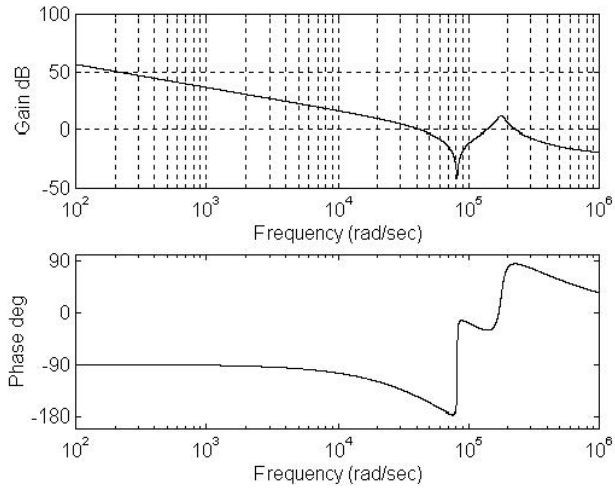

Fig. 7. W-domain Bode diagram of PFC current loop controlled object

In order that the cutoff frequency of the open loop of the corrected PFC current loop is 5 kHz=$3.14 \cdot 10^4$ rad/s, the open loop gain can be set $K = 6400$. Based on the bilinear transformation method $G(w)$ will be transformed from the W domain to the Z domain as

$$G(z) = \frac{0.6867 - 1.0839z^{-1} + 0.4277z^{-2}}{1 - 1.6186z^{-1} + 0.6186z^{-2}}. \tag{16}$$

After the correction of the Z domain for the PFC current ring open loop transfer function, the Bode diagram is shown in Fig. 8. From the graph we can see that the frequency of the first pass through the 0 dB line in the amplitude-frequency curve of the open loop transfer function is 4.89 kHz=$3.071 \cdot 10^4$ rad/s. The phase margin is 33.26°. In the simulation results, at the position of 16 kHz of the amplitude frequency curve, there are two crossing phenomena, the phase margin is negative in the position of two crossings, which will pose a threat to the stability of the module. In order to facilitate the preparation of the control program, $G(z)$ using a differential equation form is

$$I_{\mathrm{c}}(k) = 1.6186I_{\mathrm{c}}(k-1) - 0.6186I_{\mathrm{c}}(k-2) + 0.6867I_{\mathrm{e}}(k) -$$

$$- 1.0839I_{\mathrm{e}}(k-1) + 0.4277I_{\mathrm{e}}(k-2). \tag{17}$$

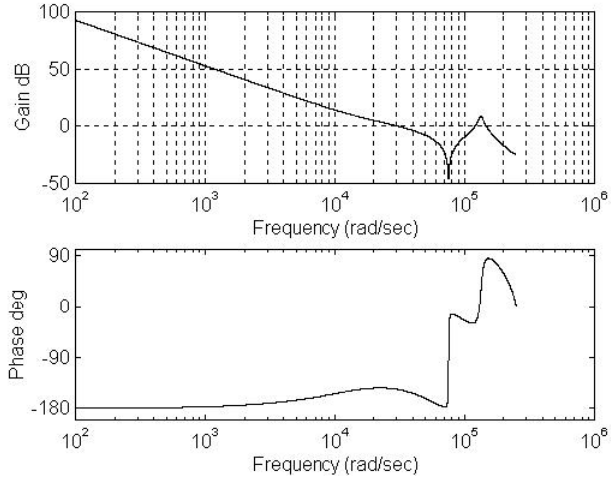

Fig. 8. Z-domain Bode diagram of PFC current loop open loop transfer function

Since the TMS320LF2406 is a 16bit DSP chip, in order to avoid overflow in the calculation, the coefficients in the differential equation are calibrated using Q10.

When the AC Source is 4 kVA, the PFC current loop is tested. The test conditions are as follows: the injection resistance is 100 Ω, sweep signal amplitude is 3 mV, the average number of times is 4, sweep speed is medium, and the frequency test range is 100 Hz–200 kHz.

The test results show that in the 220 V DC input, 15 A output, PFC inductor current is in the DCM state and the bandwidth of the PFC current loop is narrower than that of the CCM mode, only 763 Hz. The 180 V DC input, 15 A output, PFC inductor current is close to the CCM state and PFC current loop bandwidth will increase to 3.176 kHz.

2.3. PFC voltage circuit design

PFC current inner loop and power stage form a current source, while the controlled object of PFC voltage loop at low frequencies is equivalent to a current source for driving capacitor. The S-domain dynamic block diagram of the PFC voltage loop is shown in Fig. 9, in which P_{in} is the average input power of the PFC circuit, V_{O} is the output DC voltage, C is the output capacitor, and G is the voltage loop controller of PFC.

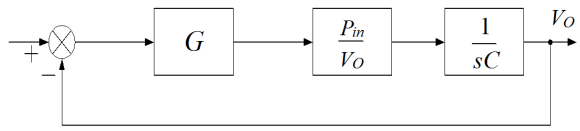

Fig. 9. S-domain dynamic block diagram of the PFC voltage loop

Under the premise of ensuring the stability of the PFC voltage loop, the bandwidth should be low enough to reduce the modulation effect of the 100 Hz voltage ripple on the PFC output capacitor to the PFC input current, otherwise the modulation will cause serious distortion of the input current.

The PFC voltage signal sampling and conditioning circuit scheme is shown in Fig. 10 (Fig. 2 comprehensively shows that the circuit uses a resistor divider to make sure that the output voltage is less than 3 V). A first-order RC filter with a cutoff frequency of 288 Hz is used to filter the high frequency noise. The voltage follower formed by LM2904 completes following and isolating, in order to enhance the output capacity of the circuit. Then in the AD port it adopts second-order RC filters with a cut-off frequency 33 kHz.

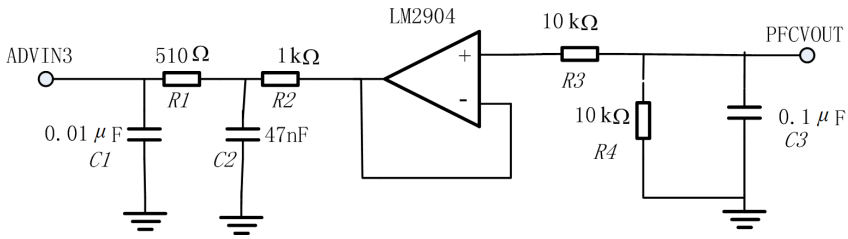

Fig. 10. Sampling circuit for PFC voltage signal

Through the analysis, (ignoring the second-order RC filter with a cut-off frequency 33 kHz in the AD port) we can see that the transfer function of the PFC voltage signal sampling circuit is

$$H(S) = \frac{0.00556}{0.5536 \cdot 10^{-3} S + 1}. \tag{18}$$

In the PFC voltage signal of AD sampling port, 3 V analog signal corresponds to the digital signal 1023, while in the PFC voltage loop controller output port the digital signal 2032 stands for "1". In order to further reduce the modulation effect of the 100 Hz voltage ripple on the PFC output capacitance to the PFC input current, the sampling value of the PFC output voltage is filtered by a first-order digital low-pass, and the cutoff frequency of the filter is 30 Hz. The filter in the W domain is expressed as

$$F(w) = \frac{1}{\left(\frac{w}{2\pi * 30} + 1\right)}. \tag{19}$$

At the calculation frequency of 20 kHz, $F(w)$ is transformed from the W domain to $F(z)$ in the Z domain, based on the bilinear transformation method.

$$F(z) = \frac{0.0047 + 0.0047 z^{-1}}{1 - 0.9906 z^{-1}}. \tag{20}$$

All the coefficients in the first-order digital low-pass filter are calibrated by the Q16 in the program.

After a comprehensive analysis, the discrete dynamic block diagram of the PFC voltage loop is shown in Fig. 11. Here T is the calculation frequency of the PFC voltage loop. At the frequency of 20 kHz, Z transform is used in the open loop transfer function of the block diagram in addition to the $G(z)$ and the digital low-pass filter, getting $P(z)$ as follows

$$P(z) = \frac{0.1054 \cdot 10^{-4} z^{-1} + 0.1023 \cdot 10^{-4} z^{-2}}{1 - 1.9136 z^{-1} + 0.9136 z^{-2}} . \tag{21}$$

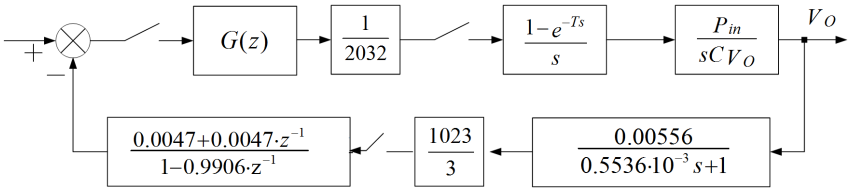

Fig. 11. Discrete dynamic block diagram of the PFC

Based on the bilinear transformation method, $P(z)$ is transformed from the Z domain to the W domain. The Bode diagrams of the W domain controlled object are shown in Figs. 12 and 13.

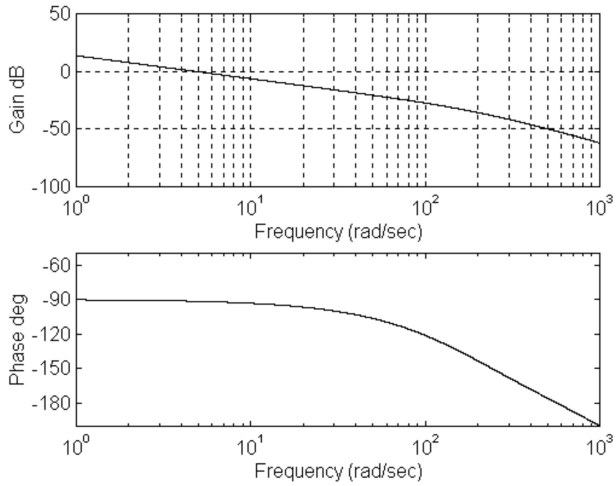

Fig. 12. Controlled object Bode diagram of W domain PFC voltage loop

The cutoff frequency of the open loop transfer function after adjustment of the PFC voltage is 12 Hz= 75.36 rad/s, and due to in digital control inherent delay there exists delay of about a calculation cycle time. The phase lag was introduced at frequency 12 Hz but as its value is small, it can be ignored. In order to get enough phase margin in the cutoff frequency of the PFC voltage loop, the controller of the PFC voltage loop adopts PI regulator, zero point is set to 2 Hz, and the controller

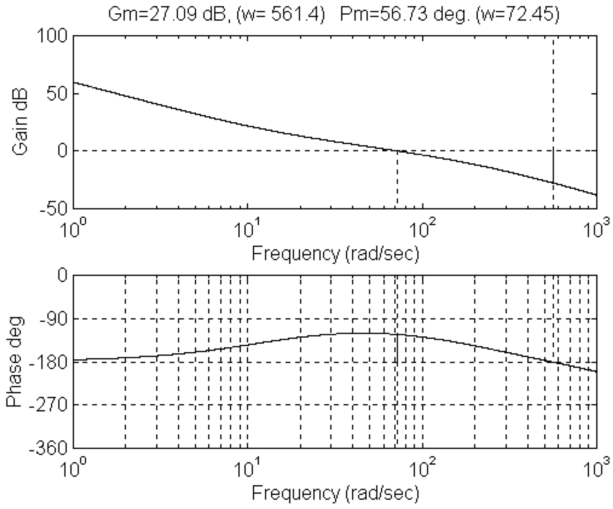

Fig. 13. Open loop transfer function Bode diagram of Z domain PFC voltage loop

structure of the W domain voltage loop is as follows

$$G(w) = \frac{K * \left(\frac{w}{2\pi * 2} + 1\right)}{w} . \tag{22}$$

In order to make the cutoff frequency of the open loop transfer function of the corrected PFC voltage loop 12 Hz= 75.36 rad/s, the open loop gain can be set $K = 200$. Based on the bilinear transformation method $G(w)$will be transformed from the W domain to the Z domain as

$$G(z) = \frac{15.9205 - 15.9105 z^{-1}}{1 - z^{-1}} . \tag{23}$$

Open loop transfer function Bode diagram of the corrected Z domain PFC voltage ring is shown in Fig. 14. The diagram shows that the amplitude cross-over frequency of the open loop transfer function is 11.5 Hz = 72.45 rad/s, the phase margin is 56.73°, and the gain margin is 27.09 dB.

In order to facilitate the preparation of control procedures and reduce the impact of truncation error, the PI controller uses the position algorithm, where the differential equations adopted are expressed in the form of

$$\mathrm{PI}(k) = \mathrm{PI}(k-1) + K_\mathrm{I} V_\mathrm{e}(k) , \tag{24}$$

$$V_\mathrm{c}(k) = K_\mathrm{P} V s_\mathrm{e}(k) + \mathrm{PI}(k) , \tag{25}$$

where

$$K_\mathrm{P} + K_\mathrm{I} = 15.9205 , \tag{26}$$

and, particularly

$$K_\mathrm{P} = 15.9105 , \quad K_\mathrm{I} = 0.01 , \tag{27}$$

All the coefficients in the first-order digital low-pass filter are calibrated by the Q16 in the program.

Adopting AC source 4 kVA for the DC power supply, the PFC voltage loop is tested. The test conditions as follows: the injection resistance is 1 k and the amplitude of sweep signal is 1 V, the average number of times is 16, the sweep speed is "Long", the frequency test range is 10 Hz–100 kHz. The experimental results show that the voltage has reached the design requirements.

3. Conclusion

In this research, the Boost PFC circuit based DSP control is studied, and the parameter selection of the main circuit is given. The design scheme and control flow of current loop and voltage loop are proposed for digital control, and an experimental prototype is designed. The actual measured results show that the input voltage is well tracked by the input current and the power factor is 0.99 at full load. Use of the DSP control parameter adjustment is more convenient, the system upgrade is easier and not easy to be influenced by aging and temperature drift. The number of devices is reduced and the anti-interference ability of the system is increased.

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